SPECIFICATION FOR COLOUR STN-LCM

(PRELIMINARY)

MODEL NO. TM128160DKFWF

TIANMA MICROELECTRONICS CO. LTD

深圳天马微电子股份有限公司

Ver. 1.0

REVISION RECORD

Date	Ver.	Ref. Page	Revision No.	Revision Item

CONTENTS

1. Display characteristics

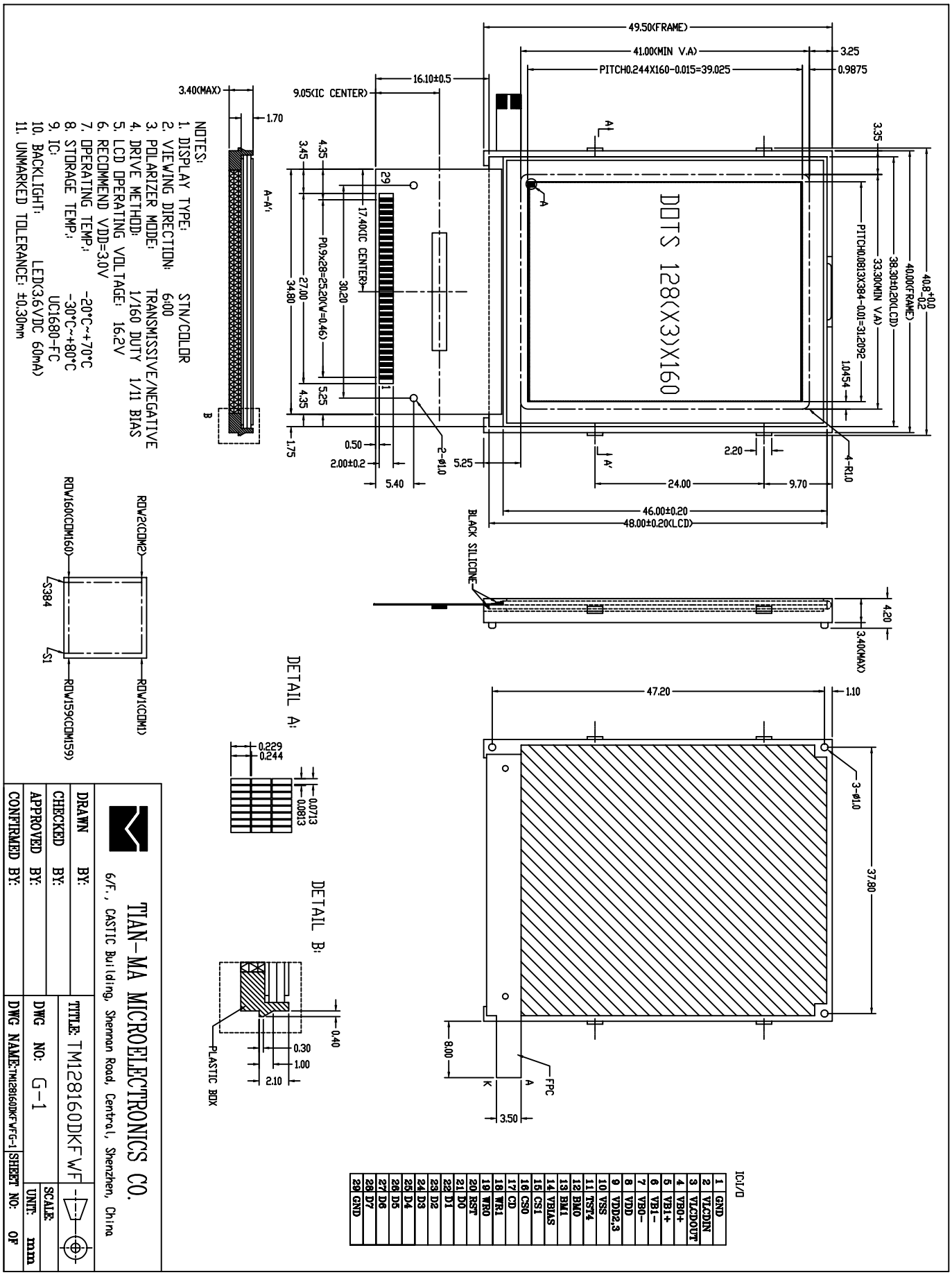
Parameter	Specification
Resolution	128*(RGB)(W)*160(H)
Illumination mode	Transmissive
Number of colors	65k
Number of gray scales	32
Normally white or black	black
Viewing direction	6:00
Backlight and color	LED,WHITE
Duty ratio	1/160
Application	MOBILE PHONE

2. Mechanical description

(1) Mechanical data

Parameter	Specifications	UNIT
Construction	COF	/
Overall dimension	40.8x49.5x3.4	mm
Viewing area	33.3x41.0	mm
Active area	31.2092x39.025	mm
Number of dots	128x3x160	Dots
Dot pitch	0.0813x0.244	mm
Dot size	0.0713x0.229	mm

(2) Outline dimensions



IC1/D	
1	GND
2	VLCDIN
3	VLCDOUT
4	VB0+
5	VB1+
6	VB1-
7	VB0-
8	VDD
9	VDD2,3
10	VSS
11	TST4
12	BM0
13	BM1
14	VBIAS
15	CS1
16	CS0
17	CD
18	WR1
19	WR0
20	RST
21	D0
22	D1
23	D2
24	D3
25	D4
26	D5
27	D6
28	D7
29	GND

3.Limiting values (absolute maximum rating system)

Subclause	Parameters	Symbol	Value		Unit
			Min.	Max.	
3.1	Operating ambient temperature	*T*op	-20	70	℃
3.2	Storage temperature	*T*stg	-30	80	℃
3.3	Supply voltage(s) (select either the pair of 3.3.1 and 3.3.2 or 3.3.3				
3.3.1	Supply voltage for logic drive	V_{DD}-V_{SS}	-0.3	4.0	V
3.3.2	Supply voltage for LCD drive	V_{DD}-V_{EE} or V_{EE}-V_{SS} or V_{DD}-V_o or V_O-V_{SS}	-0.3	18.0	V
3.3.3	Supply voltage(s) for module	V_{MDL} or $V_{MDL1,}$ $V_{MDL2,}$etc.	-0.3	4.0	V
3.4	Input signal voltage	V_{IN}	-0.4	V_{DD}+0.3	V
3.5	Voltage of integrated light source (where appropriate)			4.0	V
3.6	Operation humidity		20	65	%RH
	Storage humidity		10	80	%RH

4. Operating range and electrical and optical characteristics

4.1 Recommended operating range

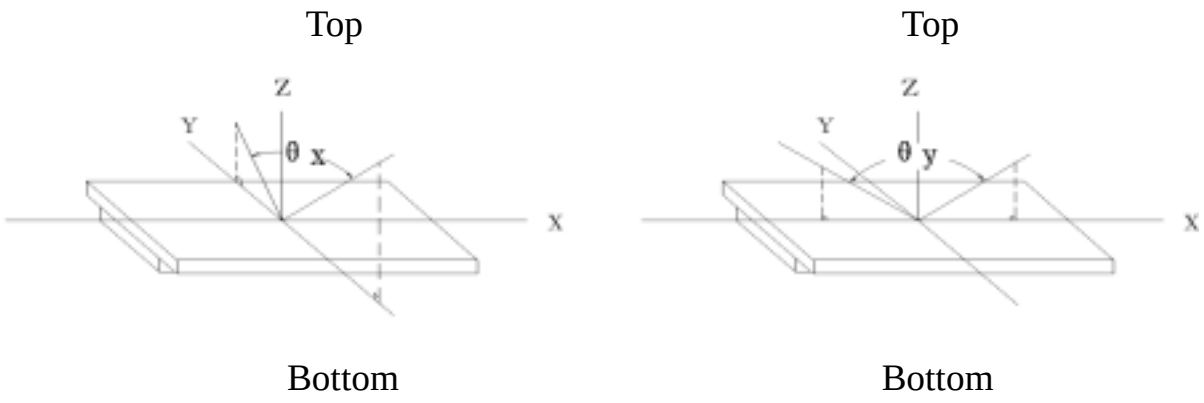
Subclause	Parameters (Characteristics at Top=25℃ unless otherwise spectified)	Symbol	Value		Unit
			Min.	Max.	
4.1.1	Operating voltage range of supply voltage(s) (select either the pair of 4.1.1and 4.1.2,or 4.1.3)				
4.1.1.1	Supply voltage for logic drive	V_{DD}-V_{SS}	1.8	3.3	**V**
4.1.1.2	Supply voltage for LCD drive	V_{DD}-V_{EE} Or V_{EE}-V_{SS} Or V_{DD}-V_O Or V_O-V_{SS}	-	-	**V**
4.1.1.3	Supply voltage(s) for module	V_{MDL} Or V_{MDL1},V_{MDL2},etc	2.4	3.3	**V**
4.1.2	Operating voltage range of input signal voltages	V_{IN}			
4.1.2.1	Input signal voltage,high	V_{INH}	$0.8V_{DD}$	V_{DD}	V
4.1.2.2	Input signal voltage,low	V_{INL}	-0.3	$0.2V_{DD}$	**V**
4.1.3	Operating voltage range of analogue light source(where appropriate)		3.3	3.7	V
4.1.4	Operating frequency range(s) (where appropriate)	F_{OP}			Hz
4.1.4.1 and/or	Operating frame frequency range	f_{FRM}	-	-	Hz
4.1.4.2	Oscillator frequency range(Line rate)	f_{OSC}	28	36	KHz

4.2 Electrical and optical characteristics

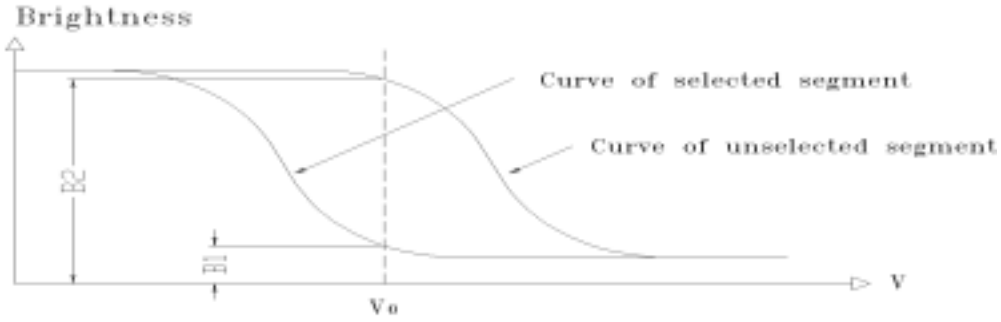
Subclasses	Characteristics at Top=25℃ unless otherwise specified	Symbol	Unit	Value	
				Min.	Max.
4.2.1	Supply current at specified frame frequency, specified operating supply voltage, with an adequate display pattern and other electrical driving conditions chosen in order to achieve extreme supply current	I_{tot} or I_{DD} and/or I_{EE}	mA		2.5
4.2.2	Operating current of integrated light source at its specified operating voltage(where appropriate)	(optional) /cs	mA		60
4.2.3	Contrast ratio :Top=25℃ , θx=0, θy=0 VLCD=Vop	CR_{dir} and/or CR_{diff}		15	
4.2.4.1	Operating display luminance at specified viewing direction and measuring point(s) (where appropriate)	L	cd/m2	65	
4.2.4.2	Luminance uniformity (where appropriate)	L_{uni}	%		60
4.2.5	Viewing angle range (Cr≥2.0)	θ_x and θ_y	deg deg	-40 -30	35 30
4.2.6.1	Rise time at 25℃	t_{on}	ms		200
4.2.6.2	Fall time at 25℃	t_{off}	ms		200
4.2.8.1	Chromaticity of white (x, y) (where appropriate)	X_W,Y_W	-	TBD	-
4.2.8.2	Chromaticity of red (x, y) (where appropriate)	X_R,Y_R	-	TBD	-
4.2.8.3	Chromaticity of blue (x,y) (where appropriate)	X_B,Y_B	-	TBD	-
4.2.8.4	Chromaticity of green (x, y) (where appropriate)	X_G,Y_G	-	TBD	-

4.3 Definition of optical characteristics

4.3.1 Definition of Viewing Angle



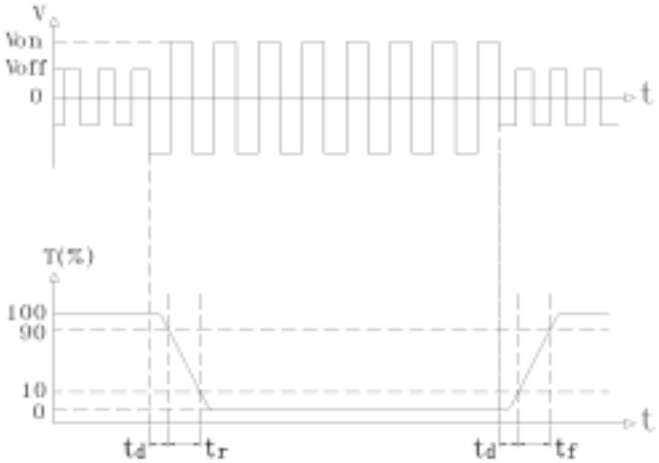
4.3.2 Definition of contrast ratio



$$\text{Contrast Ratio} = B2/B1 = \frac{\text{unselected state brightness}}{\text{selected state brightness}}$$

Measuring Conditions:

1) Ambient Temperature: 25℃ 2) Frame frequency: 70.0Hz



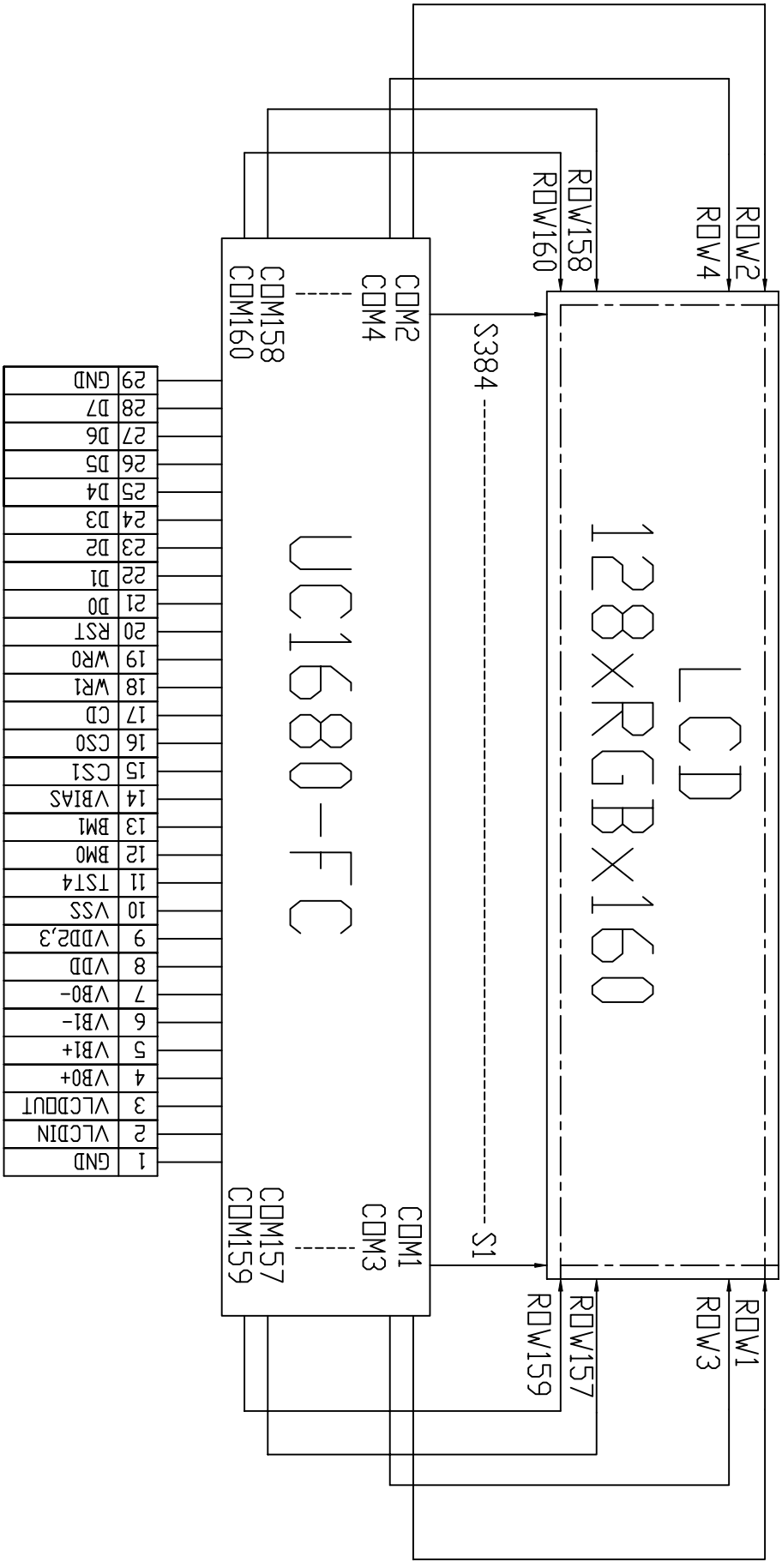
4.3.3 Definition of Response time

Turn on time: $t_{on} = t_d + t_r$ Turn off time: $t_{off} = t_d + t_f$

Measuring Condition:

1) Operating Voltage: 16.2V 2) Frame frequency: 70.0Hz

5. Circuit block diagram



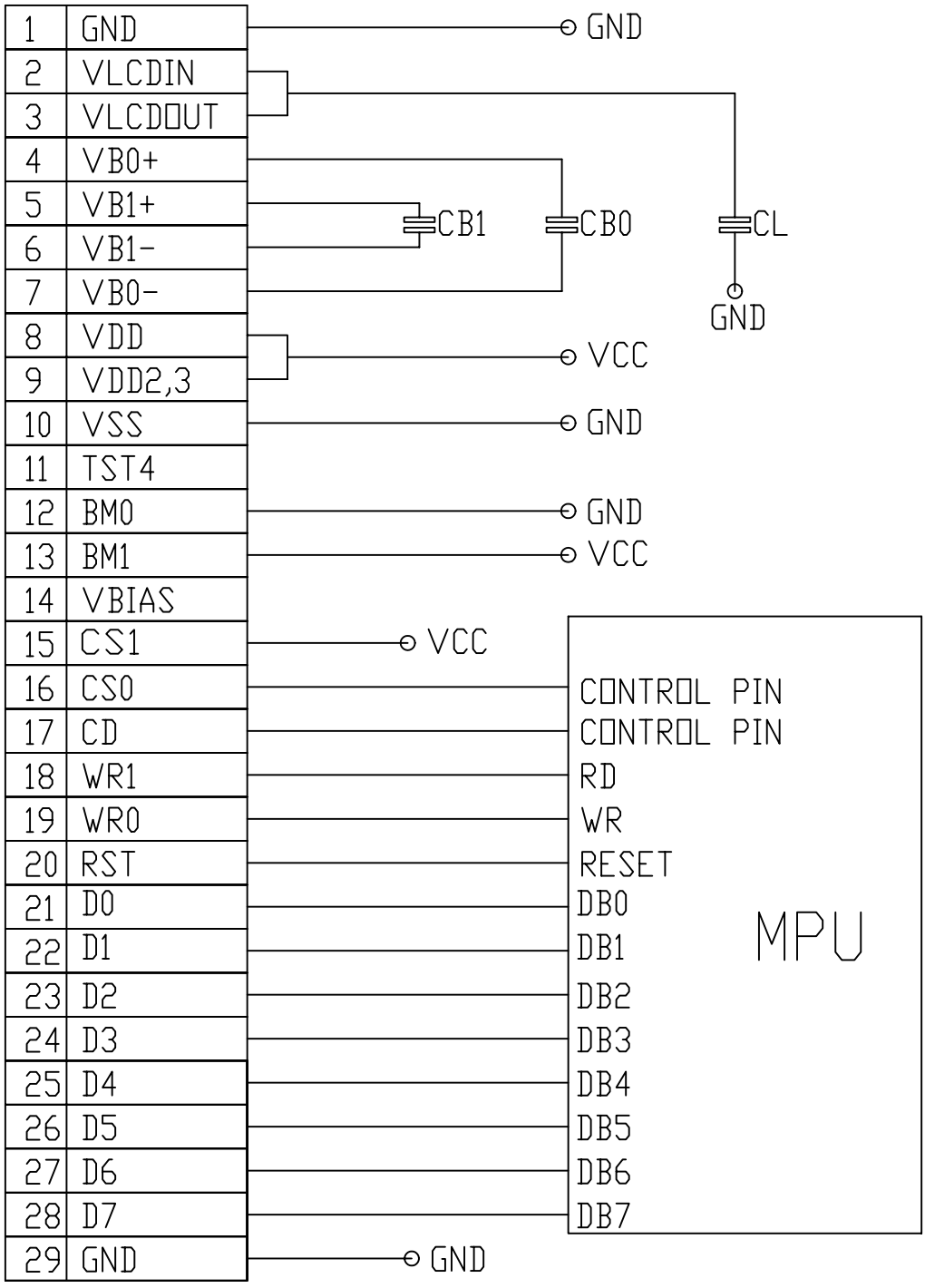
6. Interface signal

6.1 Pin Assignment

I/O:

Pin No.	Symbol	Level	Description
1	GND	0V	Ground
2	VLCDIN	-	High voltage LCD Power Supply.
3	VLCDOUT	-	Connect these pins together.
4	VB0+	-	LCD Bias Voltages.
5	VB1+	-	Connect capacitors of CBX value between VB1+ and
6	VB1-	-	VB1–, And connect capacitors of CBX value between
7	VB0-	-	VB0+ and VB0–
8	VDD	3.0V	Digital power supply
9	VDD2,3	3.0V	Analog power supply
10	VSS	0V	Ground
11	TST4	-	Leave it open during normal operation
12	BM0	H/L	The interface bus mode is determined by
13	BM1	H/L	BM[1:0]
14	VBIAS	-	Leave it open during normal use
15	CS1	H/L	Chip Select. Chip is selected when CS1=”H”
16	CS0	H/L	and CS0 = “L”
17	CD	H/L	Command or Data select pin, ”L”: Control data ”H”: Display data
18	WR1	H/L	WR[1:0] controls the read/write operation of
19	WR0	H/L	the host interface
20	RST	H/L	Reset Signal. L:Active
21	D0	H/L	Data bit0
22	D1	H/L	Data bit1
23	D2	H/L	Data bit2
24	D3	H/L	Data bit3
25	D4	H/L	Data bit4
26	D5	H/L	Data bit5
27	D6	H/L	Data bit6
28	D7	H/L	Data bit7
29	GND	0V	Ground

6.2 Example of Power Supply Circuit(8080 Mode)



CB:5uF 2.0V CL:20nF 18.0V
VCC:2.4--3.3V

7. Interface Timing Chart

AC CHARACTERISTICS

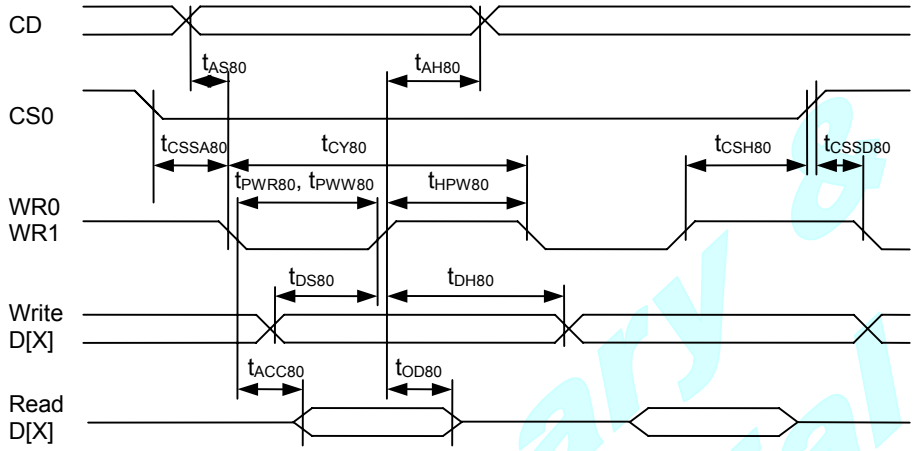


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 10	–	ns
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 128 128 128	–	ns
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits		65 35	–	ns
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits		35 35	–	ns
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 35 35	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	50 50	ns
t_{SSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 10	–	ns
t_{CY80}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 210 120 120 120	–	ns
t_{PWR80}	WR1	Pulse width 8 bits (read) 4 bits (read)		100 55	–	ns
t_{PWW80}	WR0	Pulse width 8 bits (write) 4 bits (write)		55 55	–	ns
t_{HPW80}	WR0, WR1	High pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 100 55 55 55	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	- 10		ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

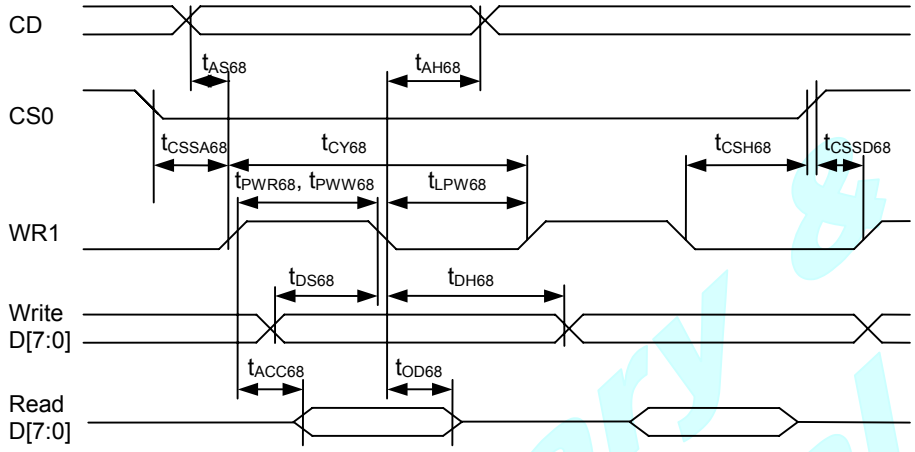


FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 10	–	ns
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 128 128 128	–	ns
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		65 35	–	ns
t_{PWW68}		Pulse width 8 bits (write) 4 bits		35 35	–	ns
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 35 35	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	50 50	ns
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 10	–	ns
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 210 120 120 120	–	ns
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		100 55	–	ns
t_{PWW68}		Pulse width 8 bits (write) 4 bits		55 55	–	ns
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 100 55 55 55	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	- 10		ns
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

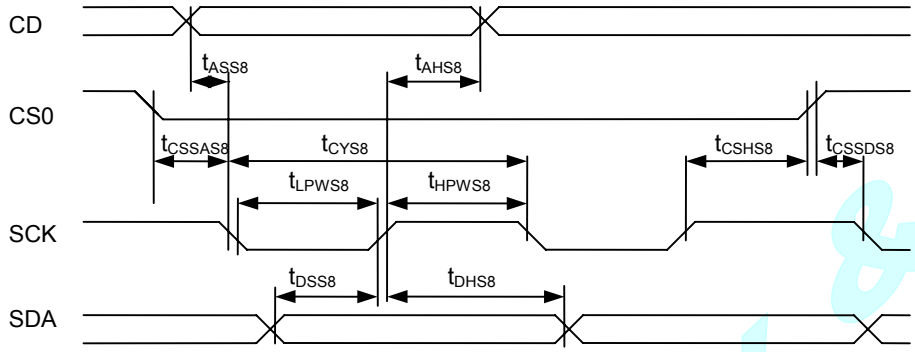


FIGURE 17: Serial Bus Timing Characteristics (for S8)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		40	–	ns
t_{CYS8}	SCK	System cycle time		135	–	ns
t_{LPWS8}		Low pulse width		65	–	ns
t_{HPWS8}		High pulse width		65	–	ns
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 10	–	ns
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	ns
t_{AHS8}		Address hold time		60	–	ns
t_{CYS8}	SCK	System cycle time		200	–	ns
t_{LPWS8}		Low pulse width		95	–	ns
t_{HPWS8}		High pulse width		95	–	ns
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 10	–	ns
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS1/CS0	Chip select setup time		10 10 20		ns

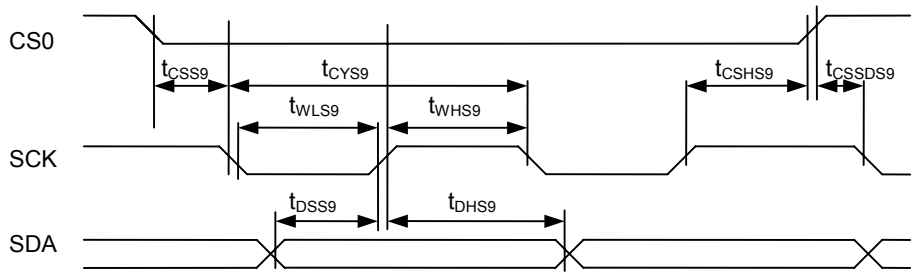


FIGURE 18: Serial Bus Timing Characteristics (for S9)

(V_{DD}=2.5V to 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		135	–	ns
t_{LPWS9}		Low pulse width		65	–	ns
t_{HPWS9}		High pulse width		65	–	ns
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 10	–	ns
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10 20		ns

(V_{DD}=1.8V to 2.5V, Ta= –30 to +85°C)

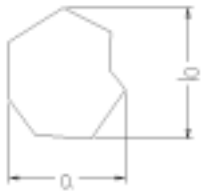
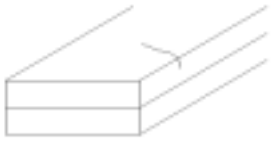
Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		200	–	ns
t_{LPWS9}		Low pulse width		95	–	ns
t_{HPWS9}		High pulse width		95	–	ns
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 10	–	ns
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS1/CS0	Chip select setup time		10 10 20		ns

8. Test of reliability Ta=25℃

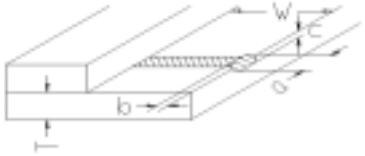
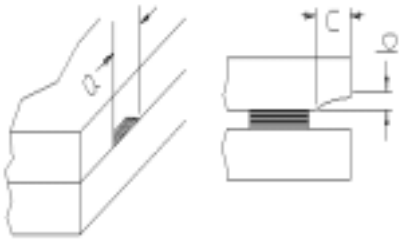
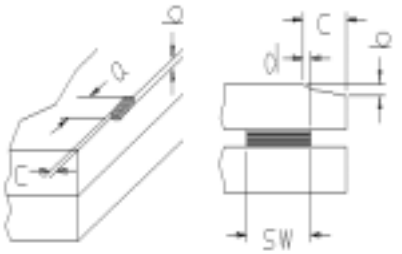
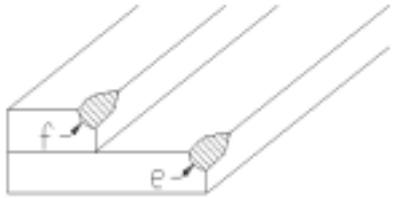
No.	Test Item	Content of Test	Test condition
1	High Temperature Storage	Endurance test applying the high storage temperature for a long time	80℃ 240H
2	Low Temperature Storage	Endurance test applying the low storage temperature for a long time	-30℃ 240H restore 4H
3	High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the thermal stress to the element for a long time	70℃ 240H
4	Low Temperature Operation	Endurance test applying the electric stress under low temperature for a long time	-20℃ 240H
5	High Temperature /Humidity Storage	Endurance test applying the high temperature and high humidity storage for a long time	60℃ 95%RH 240H
6	Temperature Cycle	Endurance test applying the low and high temperature cycle -30℃←→25℃←→80℃←→25℃ 30min 5min 30min 5min ←——————————→ 1 cycle	-30℃/80℃ 10 cycles
7	Vibration Test (package state)	Endurance test applying the vibration during transportation	10Hz~500Hz, 100m/s^2, 120min
8	Shock Test (package state)	Endurance test applying the shock during transportation	Half- sine wave, 300m/s^2, 18ms
9	Atmospheric Pressure Test	Endurance test applying the atmospheric pressure during transportation by air	25kPa 16H

9. Inspection requirement

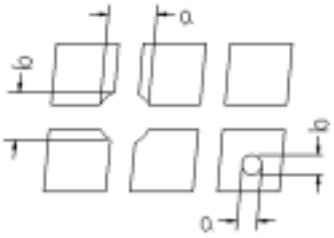
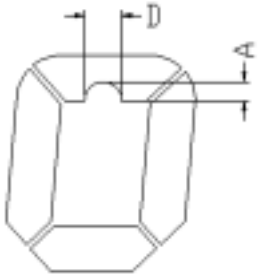
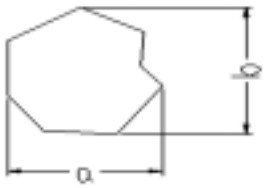
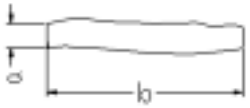
9.1 Inspection items and criteria for appearance defects

<table>
<tr><th>Items</th><th>Contents</th><th colspan="3">Criteria</th></tr>
<tr><td colspan="2">Protective Glue</td><td colspan="3">No clear defects</td></tr>
<tr><td colspan="2">Cover tape</td><td colspan="3">Covering all of the chip and no clear crimple</td></tr>
<tr><td colspan="2">Leakage</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="2">Rainbow</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td rowspan="3">Polarizer</td><td>Wrong polarizer attachment</td><td colspan="3">Not permitted</td></tr>
<tr><td rowspan="2">Bubble between polarizer and glass</td><td>Not counted</td><td colspan="2">Max. 3 defects allowed</td></tr>
<tr><td>ϕ<0.3mm</td><td colspan="2">0.3mm≤ϕ≤0.5mm</td></tr>
<tr><td>Scratches of polarizer</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td rowspan="3">Black spot (in viewing area)</td><td rowspan="3">  </td><td>Not counted</td><td>Max. 3 spots allowed</td><td rowspan="4">Max. 3 spots (lines) allowed</td></tr>
<tr><td>X<0.20mm</td><td>0.20mm≤X≤0.5mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">Black line (in viewing area)</td><td rowspan="2">  </td><td>Not counted</td><td>Max. 3 lines allowed</td></tr>
<tr><td>a<0.02mm</td><td>0.02mm≤a≤0.05mm
b≤2.0mm</td></tr>
<tr><td>Progressive cracks</td><td>  </td><td colspan="2">Not permitted</td><td></td></tr>
</table>

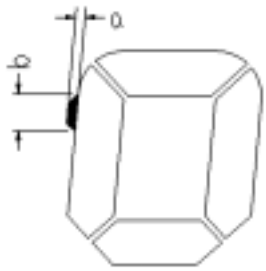
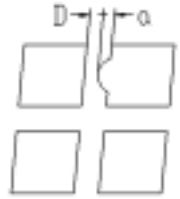
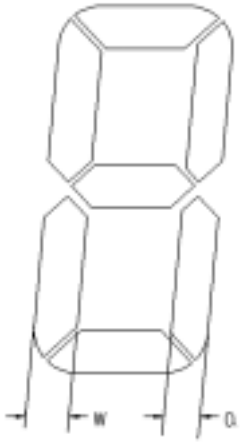
Inspection item and criteria for appearance defects (continued)

<table>
<tr><th>Items</th><th>Contents</th><th colspan="4">Criteria</th></tr>
<tr><td rowspan="4">Glass Cracks</td><td>Cracks on pads
  </td><td>a
≤3mm
≤2mm</td><td>b
≤W/5
≤W/5</td><td>c
≤T/2
T/2<C<T</td><td>Max. 2 Cracks allowed</td><td rowspan="4">Max. 5 cracks allowed</td></tr>
<tr><td>Cracks on contact side
  </td><td colspan="2">a
≤3mm
≤2mm
C shall be not reach the seal area</td><td colspan="2">b
≤T/2
T/2<b<T</td><td rowspan="3">Max. 2 cracks allowed</td></tr>
<tr><td>Cracks on non-contact side
  </td><td colspan="2">a
≤3mm
≤2mm
C≤0.5mm
d≤SW/3</td><td colspan="2">b
≤T/2
T/2<b<T</td></tr>
<tr><td>Corner cracks
  </td><td colspan="3">e<2.0mm^2
f<2.0mm^2</td><td>Max. 3 cracks allowed</td></tr>
</table>

9.2Inspection items and criteria for display defects

<table>
<tr><td colspan="2">Items</td><td>Contents</td><td colspan="3">Critera</td></tr>
<tr><td colspan="3">Open segment or open common</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Short</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Wrong viewing angle</td><td colspan="3">Not permitted</td></tr>
<tr><td colspan="3">Contrast radio uneven</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td colspan="3">Crosstalk</td><td colspan="3">According to the limit specimen</td></tr>
<tr><td rowspan="4">Pin holes and cracks in segment (DOT)</td><td rowspan="2">  </td><td>Not counted</td><td>Max.3 dots allowed</td><td rowspan="4">Max.3 dots allowed</td></tr>
<tr><td>X<0.1mm</td><td>0.1mm≤X≤0.2mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">  </td><td>Not counted</td><td>Max.2 dots allowed</td></tr>
<tr><td>A<0.1mm</td><td>0.1mm≤A≤0.2mm
D<0.25mm</td></tr>
<tr><td rowspan="3">Black spot (in viewing area)</td><td rowspan="3">  </td><td>Not counted</td><td>Max.3 spots allowed</td><td rowspan="5">Max.3 spots (lines) allowed</td></tr>
<tr><td>X<0.1mm</td><td>0.1mm≤X≤0.2mm</td></tr>
<tr><td colspan="2">X=(a+b)/2</td></tr>
<tr><td rowspan="2">Black line (in viewing area)</td><td rowspan="2">  </td><td>Not counted</td><td>Max.3 lines allowed</td></tr>
<tr><td>a<0.02mm</td><td>0.02mm≤a≤0.05mm
b≤0.5mm</td></tr>
</table>

Inspection items and criteria for display defects (continued)

<table>
<tr><th>Items</th><th>Content</th><th colspan="3">Critera</th></tr>
<tr><td rowspan="4">Transfor-
mation
of segment</td><td rowspan="2">  </td><td>Not counted</td><td>Max. 2 defects allowed</td><td rowspan="3"></td></tr>
<tr><td>x＜0.1mm</td><td>0.1mm≤x≤0.2mm</td></tr>
<tr><td colspan="2">x=(a+b)/2</td></tr>
<tr><td rowspan="2">  </td><td>Not counted</td><td>Max. 1 defects allowed</td></tr>
<tr><td>a＜0.1mm</td><td>0.1mm≤a≤0.2mm
D>0</td><td>Max.3</td></tr>
<tr><td>  </td><td colspan="3">Max.2 defects allowed
0.8W≤a≤1.2W
a=measured value of width
W=nominal value of width</td></tr>
</table>

10. Quality level

Examination or Test	At T_{amb}=25℃ (unless otherwise stated)	Inspection				
		Min.	Max.	Unit	IL	AQL
External Visual Inspection	Under normal illumination and eyesight condition, the distance between eyes and LCD is 25cm.	See 9.1			II	Major 1.0 Minor 2.5
Display Defects	Under normal illumination and eyesight condition, display on inspection.	See 9.2			II	Major 1.0 Minor 2.5
Note: Major defects: Open segment or common, Short, Serious damages, Leakage Miner defects: Others Sampling standard conforms to GB2828						

11. Precautions for Use of LCD Modules

11.1 Handling Precautions

11.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.1.6 Do not attempt to disassemble the LCD Module.

11.1.7 If the logic circuit power is off, do not apply the input signals.

11.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

a. Be sure to ground the body when handling the LCD Modules.

b. Tools required for assembly, such as soldering irons, must be properly ground.

c. To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

d. The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.2 Storage precautions

11.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃

Relatively humidity: ≤80%

11.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.3 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.